26: Advanced Operational Amplifiers - Notes

Input Resistance – The resistance measured between the two inputs of the op-amp. $R_i = 150M\Omega$

Output Resistance (Impedance) – The resistance measured between the output terminal and ground.

$R_o = 20\Omega$ (This is really an impedance at 1MHz)

Input Capacitance – The capacitance measured between the input terminals. $C_i = 2.5pF$

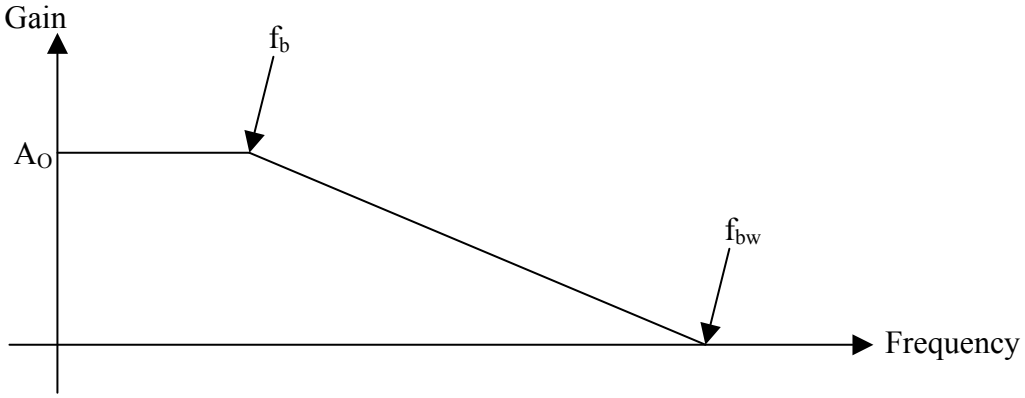
Large-Signal Voltage Gain – The gain of the op-amp alone (A_O). $A_O = A_{VD} = 100$ V/mV = 100000 V/V

Slew Rate – The maximum rate of rise or fall of the output voltage per unit time.

Positive Slew Rate = SR+ = 10V/μs
Negative Slew Rate = SR- = 13V/μs

Gain-Bandwidth (GBW)

The product of the gain and the frequency at some frequency at or higher than f_b (the 3-dB frequency) but below f_{bw}.



The gain-bandwidth is given at some frequency along the decreasing line. The gain can be found at any point along the line by assuming that the line is a straight line. The y-axis (gain) in this graph is in decibels (dB). dB = 20 log (Gain in V/V). In reverse, Gain in V/V = 10^(dB/20).

- f_b = GBW / A_O = 4MHz /100000 = 40Hz
- f_{bw} = GBW / 1 = 4MHz
- Gain at any frequency between f_b and f_{bw} = GBW / f
- Gain at any frequency below $f_b = A_O$
- Gain at frequencies above f_{bw} cannot necessarily be calculated but it is safe to assume that the gain is less than one.

As long as the estimated system gain (1/β) is less than 1/10 of the open-loop gain, A_O, at the operating frequency, the estimated system gain can be assumed to be a good estimation.

Input Voltage Limit

There are limits to the value of voltage applied to the inputs. This limit is always less than or equal to the power supply voltage. Our op-amp has its limits equal to the power supply voltages.

Input Current Limit

The current limit is set by defining the input voltage limit and the input resistance. Ohm's law gives us; Input Current Limit = Input Voltage Limit / Input Resistance.

Output Voltage Limit

The output in a typical op-amp cannot reach the level of the power supplies. For instance if the power supply voltage is +15VDC and -15VDC the maximum output voltage may be only +13VDC and -13VDC. For our op-amp, with power supply voltages at +15VDC and -15VDC, the output voltage can swing between at least -14.7V to 13.6V. However, there are op-amps available that are referred to as rail-to-rail op-amps. The output on these devices approaches a voltage very near (millivolts away) to the power supply voltage.

Output Current Limit (or the Output Short-Circuit Current)

The Output Short-Circuit Current is the maximum amount of current that can be supplied by the op-amp at the output. Many op-amps have short-circuit protection such that shorting the output to ground continuously will not harm the op-amp. Our op-amp can supply 34mA (positive output voltage) and can sink 27mA (negative output voltage).

Input Offset Voltage

If both inputs to the op-amp are tied to ground we expect that the output voltage would be zero. However due to the offset voltage at the input, the output will not be zero. The basic op-amp output voltage equation, $V_O = -A_O V_d = -A_O(V^+ - V^-)$, is altered slightly by the input offset voltage as follows, $V_O = -A_O V_d = -A_O(V^+ - V^- + V_{IO})$. Where V_{IO} is the input offset voltage. Typical input offset voltage for our op-amp is 1mV.

Input Biasing Current

Considering the voltage $(V^+ - V^-)$ at the input and the input resistance, R_i, we would expect the input current to be $(V^+ - V^-)/R_i$. Since A_O is very large and V_{out} is limited, $(V^+ - V^-)$ is effectively zero. However, the input current to each input is not zero. The input bias current is the average current flowing into the inputs for internal transistor biasing. A typical input bias current for our op-amp is 100nA.

Input Offset Current

This is the difference in input bias current from one input to the other.

Common-Mode Rejection Ratio

A common mode exists when the two inputs both have some DC voltage of the same sign. One input may have 8V and the other, 9V. They have 8V in common. The input voltage should be (V^+-V^-) = 9-8 = 1V. Unfortunately, the common DC voltage between the two inputs has a non-zero gain. The differential mode gain, A_O or A_d, magnifies the difference in the voltage between the two inputs. However, the common mode gain, A_C magnifies the common DC voltage between the two inputs. The ratio of these two gains is referred to as the Common-Mode Rejection Ratio (CMRR). This value is commonly given in dB format as follows. dB is a form of a unit. Our op-amp has a typical CMRR of 97dB.

$$CMRR = 20\log\left|\frac{A_O}{A_C}\right| dB$$

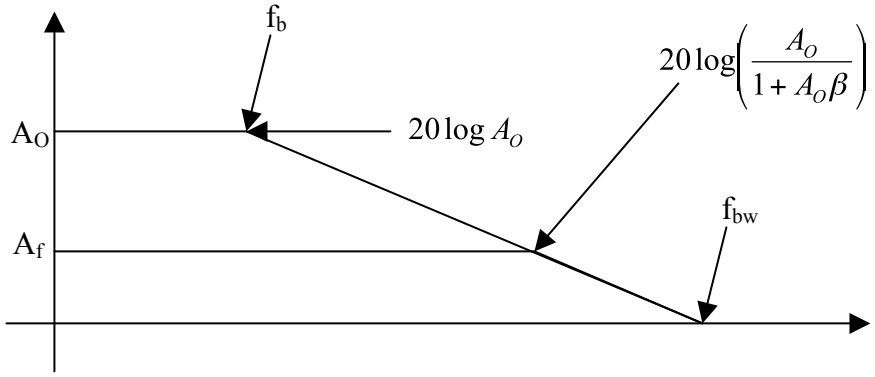
Power Supply Rejection Ratio

So far we have assumed that if the output voltage is 1.2 volts with the power supply set at 10VDC then the voltage will also be 1.2 volts with the power supply set at 12VDC. However, the value of the power supply has some effect on the output voltage. A change in the supply voltage changes the input offset voltage. The power supply rejection ratio (PSRR) is defined as the change in input offset voltage per unit change in the DC supply voltage. This is also normally given in dB. Our op-amp has a typical PSRR of 97dB although the data sheet refers to it as k_{SVR}.

$$PSRR = 20\log\left|\frac{\Delta V_{DC}}{\Delta V_{io}}\right|$$

Closed Loop Gain

Adding feedback reduces the gain from A_O to the system gain and increases the bandwidth.



You should now be prepared to answer the following questions.

1. Given the slew rate of the TLC3472, what is the rise time if the output is switching from 0V to 15V.

2. Given a gain bandwidth of 4MHz what is the op-amp gain at 1,000kHz?

3. What is the large signal voltage gain of the TLC3472?

4. What is the typical common mode gain (Ac) of the TLC3472.

5. Given power supply voltages of +12 and - 12 the input offset voltage is found to be 2.13mV. What is the expected input offset voltage of the TLC3472 (with a given PSRR of 97dB) if the power supply voltages are increased to +15 and -15?

6. True or False? The closed-loop system gain is always less than the open-loop op-amp gain.

7. The current flowing into each of the two inputs of the op-amp where measured to be 105nA and 111nA. Give the input bias current?

8. According to the TL3472 datasheet, the input offset voltage can range up to _____mV.

9. A TL3472 has power supply voltages at +15VDC and -15VDC. The closed loop gain of the system is 4V/V and the input voltage is 5VDC. What is the output voltage taking into account the output voltage limit?

10. A TL3472 has an output voltage of 10VDC and is connected to a resistor of 100 ohms. The other end of the resistor is connected to ground. What is the current that flows out of the op-amp? Be sure to take into account the output short circuit current.